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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/736,567	Applicant(s) BRENNER ET AL.	
	Examiner Clifford H Knoll	Art Unit 2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first and second paragraphs of 35 U.S.C. 112:

(1) The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

(2) The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1, 9, 10, 15, 26, 29, and 32 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 26 claims "having a first vector address executable" which is not enabled. No disclosure can be found that enables executing of addresses.

All claims recite "inserting ... into" an address, but there is no enablement of such an insertion in the specification. Note the rejection of this language under 35 USC 112(2) infra. The instant rejection under 35 USC 112(1) was deemed necessary because of possible interpretations that might arise.

Claims 1, 5, 9, 10, 13, 15, 21-23, 26, 29, and 32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, "the second interrupt mode" and "second interrupt modes" lack antecedent basis, nor is it clear their relationship to interrupt request types that are recited. "[T]he interrupt" of step (e) lacks clear antecedent basis. The "address preceding" is unclear what precedence (by priority, numerical, etc.) is intended. The step (f) is unclear because it is not clear what step is intended by the recitation of "wherein..."; apparently a means for processing is recited. If Applicant intends a processing step, the step should recite "processing...".

Also in claim 1 as well as claims 9, 10, 15, 26, 29, and 32 , "[I]nserting ... into" an address" is unclear because it is not clear how this is intended; how an address field receives an instruction, as distinct from subsequent recitation of "inserting at" of "an other instruction".

In claim 5, "the mode identifier" lacks antecedent basis.

In claim 9, the step (e) is unclear because it is not clear what step is intended by the recitation of "wherein..."; apparently a means for processing is recited. If Applicant intends a processing step, the step should recite "processing...".

In claim 13, "the mode status indicator" lacks antecedent basis.

In claim 21, "adapted for use" is unclear because it does not make clear what manner of adaptation is intended.

In claims 22 and 23, "the mode identifier" lacks antecedent basis.

In claim 32, "adapted to" is unclear because it does not make clear what manner of adaptation is intended.

For the purposes of examination, comments infra are not meant to suggest the claim language noted is indefinite, only that it is possibly broader than intended by the Applicant.

Regarding claims 1, 2, 8-10, 15, 17, 19, 22, 24, 25, 26, 29, and 32, recitation of "inserts at" an address, "that" causes a certain action (e.g., in the case of claim 1, that action is one that "disables the second interrupt mode") must be interpreted broadly. In particular, the specification in a preferred embodiment teaches a single instruction which of itself accomplishes the action. The specification also relies on the precedence of addresses in the vector table to cause the processor to execute the second instruction, in fact, in the case of the ARM processor, that vector table has only room for a single instruction, which if not a branch, will fall through to the next instruction in the vector table. Examiner is aware that Bhagat does not anticipate this particular embodiment; nonetheless Bhagat does anticipate "an instruction" that when "inserted" achieves the action that is recited. The only recitation that might serve to distinguish, the use of "preceding" is indefinite as indicated supra under 35 USC 112. There is no recitation that relates this to the instruction execution, nor is any recitation that supports the embodiment that the execution of the instruction *of itself* accomplishes the action. If Applicant's intention was a more narrow interpretation, amendment is necessary to

more narrowly recite. Otherwise, if Applicant intended the broadness of the claim (which, for example, one might infer from claim 8) additional features will be necessary to distinguish. These comments are relevant to interpretation of claim 1, but also of claims 2, 8-10, 15, 17, 19, 22, 24, 25, 26, 29, and 32.

Regarding method claims no order of precedence can be inferred unless clearly recited.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 25, 29-31 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 25 is directed to a board support package and claims 29-31 are directed to program code, all of which recite non-tangible subject matter. The claimed invention as a whole must produce a "useful, concrete and tangible" result to have a practical application (see MPEP § 2106).

Information Disclosure Statement

Applicant has satisfied requirements under 37 CFR 1.105. Reference provided by Applicant has been made of record (see attached PTO-892).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 15-18 are rejected under 35 U.S.C. 102(e) as being 15-18 by Bhagat (US 2002/0016880).

Regarding examination of claims introductory comments on claim interpretation in 35 USC 103 section, infra, should be considered.

Regarding claim 15, Bhagat discloses providing a common interrupt handler that checks a mode identifier to determine whether of first or second type (e.g., Figure 2, "204", "206"), inserting and executing another instruction that branches to the common interrupt handler (e.g., paragraph [0027]), branching to the first vector address, receiving an interrupt of the first type and setting the mode identifier to indicate an interrupt of the first type was received (e.g., Figure 3, "302"), inserting into a first vector address an instruction that disables subsequent interrupts of the first and second type (e.g., paragraph [0029]), executing an instruction to disable first and second type

interrupts (e.g., paragraph [0029]), processing the interrupt of the first type with the common interrupt dispatcher without interruptions and re-enabling first and second types (e.g., paragraph [0029]).

Regarding claim 16, Bhagat also discloses first and second types as IRQ and FIQ (e.g., Figure 2).

Regarding claim 17, Bhagat discloses providing a common interrupt handler that checks a mode identifier to determine whether of first or second type (e.g., Figure 2, "204", "206"), inserting at the second vector address and branching and executing another instruction that branches to the common interrupt handler (e.g., paragraph [0027]).

Regarding claim 18, Bhagat also discloses first and second types as IRQ and FIQ (e.g., Figure 2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-14, 19-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhagat in view of standard exception return practice for ARM processors, as

evidenced by Note 25 ("ARM application note 25: Exception handling on the ARM (including thumb-aware processors)").

Regarding claim 1, Bhagat discloses the interrupt vector table with first and second vector addresses executable, the first vector address preceding the second vector address in the vector table (e.g., paragraph [0027]), providing a common interrupt dispatcher (e.g., paragraph [0043], "common routine"), inserting an instruction into the first vector address that disables the first vector address (e.g., paragraph [0027]), inserting an other instruction that branches to the common interrupt dispatcher, providing the common interrupt dispatcher with an interrupt routine (e.g., paragraph [0026], "ISR instruction"), and re-enables the second interrupt modes, wherein requests are processed without interruption (e.g., paragraph [0027], "globally disable"). Bhagat also discloses a global enable (e.g., paragraph [0029]), but fails to expressly mention its use subsequent to processing the interrupt; however Examiner takes Official Notice that this is a standard practice in ARM interrupt processing as evidenced by the ARM Application Note. The Note discloses that interrupts are disabled and only enabled after interrupt processing (e.g., p. 22). It would be obvious to combine the Note with Bhagat because the Note discloses standard practical details of exception handling in an ARM processor which are advantageously adhered to when exception handling in an ARM processor. Therefore it would be obvious to one of ordinary skill in the art to combine Bhagat with standard practice of ARM exception handling to obtain the claimed invention.

Regarding claim 2, Bhagat also discloses inserting a single instruction that disables both interrupt modes (paragraph [0027], "globally disable").

Regarding claim 3, Bhagat also discloses re-enabling the interrupt modes (e.g., paragraph [0029]).

Regarding claim 4, Bhagat also discloses determining whether a received interrupt was the first or second type (e.g., paragraph [0031]).

Regarding claim 5, Bhagat also discloses checking the mode identifier (e.g., paragraph [0048]).

Regarding claim 6, Bhagat also discloses where an interrupt routine with an instruction branches to the first and second interrupt handlers (e.g., paragraph [0043]).

Regarding claim 7, Bhagat also discloses the IRQ and FIQ interrupt types (e.g., paragraph [0037]).

Regarding claim 8, Bhagat also discloses the single instruction (e.g., paragraph [0027], "globally disable").

Regarding claim 9, Bhagat discloses providing a common interrupt handler (e.g., paragraph [0043]), inserting into an IRQ vector address of an interrupt vector table, an instruction that disables an FIQ interrupt mode (e.g., paragraph [0028], "global disable may be enforced"), inserting at the FIQ vector address an instruction that branches to the common interrupt dispatcher (e.g., paragraph [0043]), providing the common interrupt dispatcher with an interrupt routine that processes an interrupt and re-enables the FIQ interrupt mode (e.g., paragraph [0029]), processing interrupts without interruption (e.g., paragraph [0029]). Bhagat also discloses a global enable (e.g.,

paragraph [0029]), but fails to expressly mention its use subsequent to processing the interrupt; however Examiner takes Official Notice that this is a standard practice in ARM interrupt processing as evidenced by the ARM Application Note. The Note discloses that interrupts are disabled and only enabled after interrupt processing (e.g., p. 22). It would be obvious to combine the Note with Bhagat because the Note discloses standard practical details of exception handling in an ARM processor which are advantageously adhered to when exception handling in an ARM processor. Therefore it would be obvious to one of ordinary skill in the art to combine Bhagat with standard practice of ARM exception handling to obtain the claimed invention.

Regarding claim 10, Bhagat also discloses inserting a single instruction that disables both interrupt modes (paragraph [0027], "globally disable").

Regarding claim 11, Bhagat also discloses re-enabling the interrupt modes (e.g., paragraph [0029]).

Regarding claim 12, Bhagat also discloses determining whether a received interrupt was an IRQ or an FIQ interrupt (e.g., Figure 2, "204", "206").

Regarding claim 13, Bhagat also discloses checking the mode identifier (e.g., paragraph [0031]).

Regarding claim 14, Bhagat also discloses where an interrupt routine with an instruction branches to the FIQ and IRQ interrupt handlers (e.g., paragraph [0043]; Figure 3, "310", "318").

Regarding claim 19, Bhagat discloses an instruction that disables first and second interrupt types, disposed in a first vector address of an interrupt vector table

executable upon receipt of an interrupt of the first type (e.g., paragraph [0029]), an other instruction at the second address that branches to a common interrupt handler (e.g., paragraph [0027]), a common interrupt handler that checks a mode identifier to determine whether of first or second type (e.g., Figure 2, "204", "206"), processes the interrupt and re-enables the first and second interrupt types (e.g., paragraph [0029]). Bhagat also discloses a global enable (e.g., paragraph [0029]), but fails to expressly mention its use subsequent to processing the interrupt; however Examiner takes Official Notice that this is a standard practice in ARM interrupt processing as evidenced by the ARM Application Note. The Note discloses that interrupts are disabled and only enabled after interrupt processing (e.g., p. 22). It would be obvious to combine the Note with Bhagat because the Note discloses standard practical details of exception handling in an ARM processor which are advantageously adhered to when exception handling in an ARM processor. Therefore it would be obvious to one of ordinary skill in the art to combine Bhagat with standard practice of ARM exception handling to obtain the claimed invention.

Regarding claim 20, Bhagat also discloses processing the interrupts without interruption (e.g., paragraph [0029]).

Regarding claim 21, Bhagat also discloses first and second types as IRQ and FIQ (e.g., Figure 2).

Regarding claim 22, Bhagat discloses providing the claim 21 system (e.g., Figure 2), executing a single instruction to disable IRQ and FIQ interrupts and re-enabling IRQ and FIQ interrupts (e.g., paragraph [0029]), executing an instruction to branch to the

common interrupt handler (e.g., paragraph [0027]) and processing the IRQ without interruption (e.g., paragraph [0029]) executing a single instruction receiving an IRQ interrupt, setting the mode identifier, and branching to an IRQ vector address (e.g., Figure 3, "302"). Bhagat also discloses a global enable (e.g., paragraph [0029]), but fails to expressly mention its use subsequent to processing the interrupt; however Examiner takes Official Notice that this is a standard practice in ARM interrupt processing as evidenced by the ARM Application Note. The Note discloses that interrupts are disabled and only enabled after interrupt processing (e.g., p. 22). It would be obvious to combine the Note with Bhagat because the Note discloses standard practical details of exception handling in an ARM processor which are advantageously adhered to when exception handling in an ARM processor. Therefore it would be obvious to one of ordinary skill in the art to combine Bhagat with standard practice of ARM exception handling to obtain the claimed invention.

Regarding claim 23, Bhagat discloses providing the system of claim 21 (e.g., Figure 2), receiving an FIQ interrupt, setting the mode identifier and executing the instruction at the FIQ vector to branch to the common interrupt dispatcher (e.g., Figure 2), and processing the FIQ interrupt without interruption (e.g., paragraph [0029]). Bhagat also discloses a global enable (e.g., paragraph [0029]), but fails to expressly mention its use subsequent to processing the interrupt; however Examiner takes Official Notice that this is a standard practice in ARM interrupt processing as evidenced by the ARM Application Note. The Note discloses that interrupts are disabled and only enabled after interrupt processing (e.g., p. 22). It would be obvious to combine the Note

with Bhagat because the Note discloses standard practical details of exception handling in an ARM processor which are advantageously adhered to when exception handling in an ARM processor. Therefore it would be obvious to one of ordinary skill in the art to combine Bhagat with standard practice of ARM exception handling to obtain the claimed invention.

Regarding claims 24 and 25, Bhagat discloses an instruction that disables first and second interrupt types (e.g., paragraph [0029]), an instruction that branches to a common interrupt dispatcher (e.g., paragraph [0027]), a common interrupt dispatcher that checks a mode identifier to determine whether a received interrupt was of the first or second type and processes the interrupt (e.g., paragraph [0027]). Bhagat also discloses a global enable (e.g., paragraph [0029]), but fails to expressly mention its use subsequent to processing the interrupt; however this is a standard practice in ARM interrupt processing as evidenced by the ARM Application Note. The Note discloses that interrupts are disabled and only enabled after interrupt processing (e.g., p. 22). It would be obvious to combine the Note with Bhagat because the Note discloses standard practical details of exception handling in an ARM processor which are advantageously adhered to when exception handling in an ARM processor. Therefore it would be obvious to one of ordinary skill in the art to combine Bhagat with standard practice of ARM exception handling to obtain the claimed invention.

Regarding claims 26 and 29, Bhagat discloses code for a dispatcher for a processor with first and second interrupt modes, with the second higher than the first and interrupt vector table with first and second vector addresses (e.g., paragraph

[0030]), a mode status indicator (e.g., Figure 3, "302"), code for inserting an instruction into the first vector address that disables first and second interrupts (e.g., paragraph [0029]), code for inserting an instruction that branches to a common interrupt dispatcher (e.g., paragraph [0027]), and code for providing the dispatcher with an interrupt routine that checks the mode identifier to determine which type (e.g., paragraph [0027]). Bhagat also discloses a global enable (e.g., paragraph [0029]), but fails to expressly mention its use subsequent to processing the interrupt; however this is a standard practice in ARM interrupt processing as evidenced by the ARM Application Note. The Note discloses that interrupts are disabled and only enabled after interrupt processing (e.g., p. 22). It would be obvious to combine the Note with Bhagat because the Note discloses standard practical details of exception handling in an ARM processor which are advantageously adhered to when exception handling in an ARM processor. Therefore it would be obvious to one of ordinary skill in the art to combine Bhagat with standard practice of ARM exception handling to obtain the claimed invention.

Regarding claims 27 and 30 Bhagat also discloses branches first and second interrupts to first and second handlers (e.g., Figure 3, "318", "314").

Regarding claims 28 and 31, Bhagat also discloses IRQ and FIQ (e.g., Figure 2).

Regarding claim 32, Bhagat discloses providing a processor with first and second interrupt modes to accept interrupt requests of first and second types (e.g., Figure 2, "IRQ", "FIQ"), a mode status indicator (e.g., Figure 3, "302"), code for inserting an instruction into the first vector address that disables the first and second interrupts (e.g., paragraph [0029]), a processor to execute the instruction in the interrupt table without

interruption (e.g., paragraph [0023]), providing a common interrupt dispatcher (e.g., paragraph [0027]), inserting an instruction that disables the second interrupt mode (e.g., paragraph [0029]), providing the common interrupt dispatcher with an interrupt routine that processes the interrupt and re-enables the second interrupt modes (e.g., paragraph [0029]). Bhagat also discloses a global enable (e.g., paragraph [0029]), but fails to expressly mention its use subsequent to processing the interrupt; however Examiner takes Official Notice that this is a standard practice in ARM interrupt processing as evidenced by the ARM Application Note. The Note discloses that interrupts are disabled and only enabled after interrupt processing (e.g., p. 22). It would be obvious to combine the Note with Bhagat because the Note discloses standard practical details of exception handling in an ARM processor which are advantageously adhered to when exception handling in an ARM processor. Therefore it would be obvious to one of ordinary skill in the art to combine Bhagat with standard practice of ARM exception handling to obtain the claimed invention.

Claims 1-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhagat in view of standard exception practice in ARM processors, as evidenced by Note 25, further in view of Note 31 ("ARM application note 31: Using embeddedICE").

Regarding claim 1, Bhagat discloses the interrupt vector table with first and second vector addresses executable, the first vector address preceding the second vector address in the vector table (e.g., paragraph [0027]), providing a common interrupt dispatcher (e.g., paragraph [0043], "common routine"), inserting an instruction

into the first vector address that disables the first vector address (e.g., paragraph [0027]), inserting an other instruction that branches to the common interrupt dispatcher, providing the common interrupt dispatcher with an interrupt routine (e.g., paragraph [0026], "ISR instruction"), and then re-enables the second interrupt modes, wherein requests are processed without interruption (e.g., paragraph [0027], "globally disable"). Bhagat does not expressly mention a single instruction by itself accomplishing this; however, this is disclosed by Note 31 (pp. 11-12). It would be obvious to combine Note 31 with Bhagat because Note 31 teaches specific instruction details in the vector table that allow common interrupt handling in an ARM processor, such as the common interrupt handler of Bhagat. Therefore it would be obvious to one of ordinary skill in the art to combine Note 31 with Bhagat to obtain the claimed invention.

Regarding claim 2, Bhagat also discloses inserting a single instruction that disables both interrupt modes (paragraph [0027], "globally disable"). Bhagat does not expressly mention a single instruction by itself accomplishing this; however, this is disclosed by Note 31 (e.g., p. 12, "ORR r13, r13, 0xC0").

Regarding claim 3, Bhagat also discloses re-enabling the interrupt modes (e.g., paragraph [0029]).

Regarding claim 4, Bhagat also discloses determining whether a received interrupt was the first or second type (e.g., paragraph [0031]).

Regarding claim 5, Bhagat also discloses checking the mode identifier (e.g., paragraph [0048]).

Regarding claim 6, Bhagat also discloses where an interrupt routine with an instruction branches to the first and second interrupt handlers (e.g., paragraph [0043]).

Regarding claim 7, Bhagat also discloses the IRQ and FIQ interrupt types (e.g., paragraph [0037]).

Regarding claim 8, Bhagat discloses the single instruction (e.g., paragraph [0027], "globally disable"). Bhagat does not expressly mention a single instruction by itself accomplishing this; however, this is disclosed by Note 31 (e.g., p. 12, "ORR r13, r13, 0xC0").

Regarding claim 9, Bhagat discloses providing a common interrupt handler (e.g., paragraph [0043]), inserting into an IRQ vector address of an interrupt vector table, an instruction that disables an FIQ interrupt mode (e.g., paragraph [0028], "global disable may be enforced"), inserting at the FIQ vector address an instruction that branches to the common interrupt dispatcher (e.g., paragraph [0043]), providing the common interrupt dispatcher with an interrupt routine that processes an interrupt and the re-enables the FIQ interrupt mode (e.g., paragraph [0029]), processing interrupts without interruption (e.g., paragraph [0029]).

Bhagat also discloses a global enable (e.g., paragraph [0029]), but fails to expressly mention its use subsequent to processing the interrupt; however Examiner takes Official Notice that this is a standard practice in ARM interrupt processing as evidenced by the ARM Application Note. The Note discloses that interrupts are disabled and only enabled after interrupt processing (e.g., p. 22). It would be obvious to combine the Note with Bhagat because the Note discloses standard practical details of

exception handling in an ARM processor which are advantageously adhered to when exception handling in an ARM processor. Therefore it would be obvious to one of ordinary skill in the art to combine Bhagat with standard practice of ARM exception handling to obtain the claimed invention.

Bhagat does not expressly mention a single instruction by itself accomplishing this; however, this is disclosed by Note 31 (pp. 11-12). It would be obvious to combine Note 31 with Bhagat because Note 31 teaches specific instruction details in the vector table that allow common interrupt handling in an ARM processor, such as the common interrupt handler of Bhagat. Therefore it would be obvious to one of ordinary skill in the art to combine Note 31 with Bhagat to obtain the claimed invention.

Regarding claim 10, Bhagat also discloses inserting a single instruction that disables both interrupt modes (paragraph [0027], "globally disable"). Bhagat does not expressly mention a single instruction by itself accomplishing this; however, this is disclosed by Note 31 (e.g., p. 12, "ORR r13, r13, 0xC0").

Regarding claim 11, Bhagat also discloses re-enabling the interrupt modes (e.g., paragraph [0029]).

Regarding claim 12, Bhagat also discloses determining whether a received interrupt was an IRQ or an FIQ interrupt (e.g., Figure 2, "204", "206").

Regarding claim 13, Bhagat also discloses checking the mode identifier (e.g., paragraph [0031]).

Regarding claim 14, Bhagat also discloses where an interrupt routine with an instruction branches to the FIQ and IRQ interrupt handlers (e.g., paragraph [0043]; Figure 3, "310", "318").

Regarding claim 15, Bhagat discloses providing a common interrupt handler that checks a mode identifier to determine whether of first or second type (e.g., Figure 2, "204", "206"), inserting and executing another instruction that branches to the common interrupt handler (e.g., paragraph [0027]), branching to the first vector address, receiving an interrupt of the first type and setting the mode identifier to indicate an interrupt of the first type was received (e.g., Figure 3, "302"), inserting into a first vector address an instruction that disables subsequent interrupts of the first and second type (e.g., paragraph [0029]), executing an instruction to disable first and second type interrupts (e.g., paragraph [0029]), processing the interrupt of the first type with the common interrupt dispatcher without interruptions and re-enabling first and second types (e.g., paragraph [0029]).

Bhagat also discloses a global enable (e.g., paragraph [0029]), but fails to expressly mention its use subsequent to processing the interrupt; however Examiner takes Official Notice that this is a standard practice in ARM interrupt processing as evidenced by the ARM Application Note. The Note discloses that interrupts are disabled and only enabled after interrupt processing (e.g., p. 22). It would be obvious to combine the Note with Bhagat because the Note discloses standard practical details of exception handling in an ARM processor which are advantageously adhered to when exception handling in an ARM processor. Therefore it would be obvious to one of

ordinary skill in the art to combine Bhagat with standard practice of ARM exception handling to obtain the claimed invention.

Bhagat does not expressly mention a single instruction by itself accomplishing this; however, this is disclosed by Note 31 (pp. 11-12). It would be obvious to combine Note 31 with Bhagat because Note 31 teaches specific instruction details in the vector table that allow common interrupt handling in an ARM processor, such as the common interrupt handler of Bhagat. Therefore it would be obvious to one of ordinary skill in the art to combine Note 31 with Bhagat to obtain the claimed invention.

Regarding claim 16, Bhagat also discloses first and second types as IRQ and FIQ (e.g., Figure 2).

Regarding claim 17, Bhagat discloses providing a common interrupt handler that checks a mode identifier to determine whether of first or second type (e.g., Figure 2, "204", "206"), inserting at the second vector address and branching and executing another instruction that branches to the common interrupt handler (e.g., paragraph [0027]).

Bhagat also discloses a global enable (e.g., paragraph [0029]), but fails to expressly mention its use subsequent to processing the interrupt; however Examiner takes Official Notice that this is a standard practice in ARM interrupt processing as evidenced by the ARM Application Note. The Note discloses that interrupts are disabled and only enabled after interrupt processing (e.g., p. 22). It would be obvious to combine the Note with Bhagat because the Note discloses standard practical details of exception handling in an ARM processor which are advantageously adhered to when

exception handling in an ARM processor. Therefore it would be obvious to one of ordinary skill in the art to combine Bhagat with standard practice of ARM exception handling to obtain the claimed invention.

Bhagat does not expressly mention a single instruction by itself accomplishing this; however, this is disclosed by Note 31 (pp. 11-12). It would be obvious to combine Note 31 with Bhagat because Note 31 teaches specific instruction details in the vector table that allow common interrupt handling in an ARM processor, such as the common interrupt handler of Bhagat. Therefore it would be obvious to one of ordinary skill in the art to combine Note 31 with Bhagat to obtain the claimed invention.

Regarding claim 18, Bhagat also discloses first and second types as IRQ and FIQ (e.g., Figure 2).

Regarding claim 19, Bhagat discloses an instruction that disables first and second interrupt types, disposed in a first vector address of an interrupt vector table executable upon receipt of an interrupt of the first type (e.g., paragraph [0029]), an other instruction at the second address that branches to a common interrupt handler (e.g., paragraph [0027]), a common interrupt handler that checks a mode identifier to determine whether of first or second type (e.g., Figure 2, "204", "206"), processes the interrupt and re-enables the first and second interrupt types (e.g., paragraph [0029]). Bhagat does not expressly mention a single instruction by itself accomplishing this; however, this is disclosed by Note 31 (pp. 11-12). It would be obvious to combine Note 31 with Bhagat because Note 31 teaches specific instruction details in the vector table that allow common interrupt handling in an ARM processor, such as the common

interrupt handler of Bhagat. Therefore it would be obvious to one of ordinary skill in the art to combine Note 31 with Bhagat to obtain the claimed invention.

Regarding claim 20, Bhagat also discloses processing the interrupts without interruption (e.g., paragraph [0029]).

Regarding claim 21, Bhagat also discloses first and second types as IRQ and FIQ (e.g., Figure 2).

Regarding claim 22, Bhagat discloses providing the claim 21 system (e.g., Figure 2), executing a single instruction to disable IRQ and FIQ interrupts and re-enabling IRQ and FIQ interrupts (e.g., paragraph [0029]), executing an instruction to branch to the common interrupt handler (e.g., paragraph [0027]) and processing the IRQ without interruption (e.g., paragraph [0029]) executing a single instruction receiving an IRQ interrupt, setting the mode identifier, and branching to an IRQ vector address (e.g., Figure 3, "302").

Bhagat also discloses a global enable (e.g., paragraph [0029]), but fails to expressly mention its use subsequent to processing the interrupt; however Examiner takes Official Notice that this is a standard practice in ARM interrupt processing as evidenced by the ARM Application Note. The Note discloses that interrupts are disabled and only enabled after interrupt processing (e.g., p. 22). It would be obvious to combine the Note with Bhagat because the Note discloses standard practical details of exception handling in an ARM processor which are advantageously adhered to when exception handling in an ARM processor. Therefore it would be obvious to one of

ordinary skill in the art to combine Bhagat with standard practice of ARM exception handling to obtain the claimed invention.

Bhagat does not expressly mention a single instruction by itself accomplishing this; however, this is disclosed by Note 31 (pp. 11-12). It would be obvious to combine Note 31 with Bhagat because Note 31 teaches specific instruction details in the vector table that allow common interrupt handling in an ARM processor, such as the common interrupt handler of Bhagat. Therefore it would be obvious to one of ordinary skill in the art to combine Note 31 with Bhagat to obtain the claimed invention.

Regarding claim 23, Bhagat discloses providing the system of claim 21 (e.g., Figure 2), receiving an FIQ interrupt, setting the mode identifier and executing the instruction at the FIQ vector to branch to the common interrupt dispatcher (e.g., Figure 2), and processing the FIQ interrupt without interruption (e.g., paragraph [0029]).

Bhagat also discloses a global enable (e.g., paragraph [0029]), but fails to expressly mention its use subsequent to processing the interrupt; however Examiner takes Official Notice that this is a standard practice in ARM interrupt processing as evidenced by the ARM Application Note. The Note discloses that interrupts are disabled and only enabled after interrupt processing (e.g., p. 22). It would be obvious to combine the Note with Bhagat because the Note discloses standard practical details of exception handling in an ARM processor which are advantageously adhered to when exception handling in an ARM processor. Therefore it would be obvious to one of ordinary skill in the art to combine Bhagat with standard practice of ARM exception handling to obtain the claimed invention.

Bhagat does not expressly mention a single instruction by itself accomplishing this; however, this is disclosed by Note 31 (pp. 11-12). It would be obvious to combine Note 31 with Bhagat because Note 31 teaches specific instruction details in the vector table that allow common interrupt handling in an ARM processor, such as the common interrupt handler of Bhagat. Therefore it would be obvious to one of ordinary skill in the art to combine Note 31 with Bhagat to obtain the claimed invention.

Regarding claims 24 and 25, Bhagat discloses an instruction that disables first and second interrupt types (e.g., paragraph [0029]), an instruction that branches to a common interrupt dispatcher (e.g., paragraph [0027]), a common interrupt dispatcher that checks a mode identifier to determine whether a received interrupt was of the first or second type and processes the interrupt (e.g., paragraph [0027]).

Bhagat also discloses a global enable (e.g., paragraph [0029]), but fails to expressly mention its use subsequent to processing the interrupt; however this is a standard practice in ARM interrupt processing as evidenced by the ARM Application Note. The Note discloses that interrupts are disabled and only enabled after interrupt processing (e.g., p. 22). It would be obvious to combine the Note with Bhagat because the Note discloses standard practical details of exception handling in an ARM processor which are advantageously adhered to when exception handling in an ARM processor. Therefore it would be obvious to one of ordinary skill in the art to combine Bhagat with standard practice of ARM exception handling to obtain the claimed invention.

Bhagat does not expressly mention a single instruction by itself accomplishing this; however, this is disclosed by Note 31 (pp. 11-12). It would be obvious to combine

Note 31 with Bhagat because Note 31 teaches specific instruction details in the vector table that allow common interrupt handling in an ARM processor, such as the common interrupt handler of Bhagat. Therefore it would be obvious to one of ordinary skill in the art to combine Note 31 with Bhagat to obtain the claimed invention.

Regarding claims 26 and 29, Bhagat discloses code for a dispatcher for a processor with first and second interrupt modes, with the second higher than the first and interrupt vector table with first and second vector addresses (e.g., paragraph [0030]), a mode status indicator (e.g., Figure 3, "302"), code for inserting an instruction into the first vector address that disables first and second interrupts (e.g., paragraph [0029]), code for inserting an instruction that branches to a common interrupt dispatcher (e.g., paragraph [0027]), and code for providing the dispatcher with an interrupt routine that checks the mode identifier to determine which type (e.g., paragraph [0027]).

Bhagat also discloses a global enable (e.g., paragraph [0029]), but fails to expressly mention its use subsequent to processing the interrupt; however this is a standard practice in ARM interrupt processing as evidenced by the ARM Application Note. The Note discloses that interrupts are disabled and only enabled after interrupt processing (e.g., p. 22). It would be obvious to combine the Note with Bhagat because the Note discloses standard practical details of exception handling in an ARM processor which are advantageously adhered to when exception handling in an ARM processor. Therefore it would be obvious to one of ordinary skill in the art to combine Bhagat with standard practice of ARM exception handling to obtain the claimed invention.

Bhagat does not expressly mention a single instruction by itself accomplishing this; however, this is disclosed by Note 31 (pp. 11-12). It would be obvious to combine Note 31 with Bhagat because Note 31 teaches specific instruction details in the vector table that allow common interrupt handling in an ARM processor, such as the common interrupt handler of Bhagat. Therefore it would be obvious to one of ordinary skill in the art to combine Note 31 with Bhagat to obtain the claimed invention.

Regarding claims 27 and 30 Bhagat also discloses branches first and second interrupts to first and second handlers (e.g., Figure 3, "318", "314").

Regarding claims 28 and 31, Bhagat also discloses IRQ and FIQ (e.g., Figure 2).

Regarding claim 32, Bhagat discloses providing a processor with first and second interrupt modes to accept interrupt requests of first and second types (e.g., Figure 2, "IRQ", "FIQ"), a mode status indicator (e.g., Figure 3, "302"), code for inserting an instruction into the first vector address that disables the first and second interrupts (e.g., paragraph [0029]), a processor to execute the instruction in the interrupt table without interruption (e.g., paragraph [0023]), providing a common interrupt dispatcher (e.g., paragraph [0027]), inserting an instruction that disables the second interrupt mode (e.g., paragraph [0029]), providing the common interrupt dispatcher with an interrupt routine that processes the interrupt and re-enables the second interrupt modes (e.g., paragraph [0029]).

Bhagat also discloses a global enable (e.g., paragraph [0029]), but fails to expressly mention its use subsequent to processing the interrupt; however Examiner takes Official Notice that this is a standard practice in ARM interrupt processing as

evidenced by the ARM Application Note. The Note discloses that interrupts are disabled and only enabled after interrupt processing (e.g., p. 22). It would be obvious to combine the Note with Bhagat because the Note discloses standard practical details of exception handling in an ARM processor which are advantageously adhered to when exception handling in an ARM processor. Therefore it would be obvious to one of ordinary skill in the art to combine Bhagat with standard practice of ARM exception handling to obtain the claimed invention.

Bhagat does not expressly mention a single instruction by itself accomplishing this; however, this is disclosed by Note 31 (pp. 11-12). It would be obvious to combine Note 31 with Bhagat because Note 31 teaches specific instruction details in the vector table that allow common interrupt handling in an ARM processor, such as the common interrupt handler of Bhagat. Therefore it would be obvious to one of ordinary skill in the art to combine Note 31 with Bhagat to obtain the claimed invention.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. "Atmel AT91 ARM thumb microcontrollers application note: Disabling interrupts at processor level" provide specific instructions for disabling interrupts. Nevill (US 2002/0099933) provides additional comments on disabling FIQ and IRQ interrupts.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H Knoll whose telephone number is 703-305-8656. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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